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37 L1

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Search Results -

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L2 710/5,36,62,63,100,300;711/113,114,130,118,112,148,141;714/5,7,9;700/2;370/363,452.ccls. 12170 L2

L1 (storage or memory or disk or disc) same ((intercontroller or (inter adj1 controller)) same link) 37 L1

END OF SEARCH HISTORY

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Search Results -

Terms	Documents
L1 and L2	23

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR

L3 11 and L2

23 L3

L2 710/5,36,62,63,100,300;711/113,114,130,118,112,148,141;714/5,7,9;700/2,370/363,452.ccls.

12170 L2

L1 (storage or memory or disk or disc) same ((intercontroller or (inter adj1 controller)) same link)

37 L1

END OF SEARCH HISTORY



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controller)) same link)

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	U	1	Document ID	Issue Dat	Pages	Title	Current OR	Current X
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6912629	20050628	12	System and method for	711/161	711/162
			B1			restoring data from sec		
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6883065	20050419	29	System and method for a	711/114	709/206;
			B1			redundant communication		709/207;
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6658590	20031202	26	Controller-based	714/6	714/15;
			B1			transaction loading svcs		714/20
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6658540	20031202	29	Method for transaction	711/162	707/204;
			B1			command ordering in a r		711/161
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6647474	20031111	15	Remote data mirroring	711/162	711/161;
			B2			system using local and		711/165;
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6643795	20031104	30	Controller-based	714/6	714/11;
			B1			bi-directional remote c		714/13;
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6629264	20030930	31	Controller-based remote	714/15	714/18
			B1			conv svstem with logica		
8	<input type="checkbox"/>	<input type="checkbox"/>	US 6629158	20030930	12	System, apparatus, and	710/10	710/104;
			B1			method for configuring		710/15;
9	<input type="checkbox"/>	<input type="checkbox"/>	US 6625705	20030923	17	Remote data mirroring	711/162	711/161;
			B2			system having a service		711/165;
10	<input type="checkbox"/>	<input type="checkbox"/>	US 6502205	20021231	58	Asynchronous remote	714/7	714/718
			B1			data mirroring svstem		
11	<input type="checkbox"/>	<input type="checkbox"/>	US 6446175	20020903	18	Storing and retrieving	711/162	711/161



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IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

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1. A four station controller area network

Boyce, C.R.;

Vehicle Networks for Multiplexing and Data Communication, IEE Colloquium on 19 Dec 1988 Page(s):9/1 - 9/7

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2. Resource management in an integrated optical network

Sohraby, K.; Zhensheng Zhang; Xiaowen Chu; Bo Li;

Selected Areas in Communications, IEEE Journal on Volume 21, Issue 7, Sept. 2003 Page(s):1052 - 1062

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Resource management in an integrated optical network

Sohraby, K., Zhensteng Zhang, Xiaowen Qiu, Bo Li
Bell Labs, Holmdel, NJ, USA

This paper appears in: **Selected Areas In Communications, IEEE Journal on**

Publication Date: Sept. 2003

Volume: 21, Issue: 7

On page(s): 1052 - 1062

ISSN: 0733-8716

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Abstract

We propose a novel integrated optical network switching architecture. The proposal offers an approach to signaling for the purpose of transport on an all-optical network of optical and nonoptical legacy network traffic. In order to provide effective end-to-end control and efficient transport services, new signaling and control techniques are required. Standard organizations such as Optical Interworking Forum (OIF) and Internet Engineering Task Force have developed interface methods between client and transport networks, as well as signaling processes for resource allocation. We propose a network controller, which implements interfaces for such integration in the intermediate future, as well as provides a feasible path for the long-term objective of all optical networking. Performance and capacity issues for these systems introduce new dimensions to the existing set of networking problems, since optical paths can now be set up in real-time. There are two main contributions in this paper: (1) functional composition of a network controller, which translates legacy signaling to optical connection signaling and path establishment and (2) determining when to issue an optical connection request based on the current network conditions such as link utilization, so that the integrated optical network can operate efficiently. Analytical approximations, as well as simulation results for call blocking performance are also presented.

Index Terms
Inspec

Controlled Indexing

optical fibre networks standardisation telecommunication congestion control telecommunication control
telecommunication network management telecommunication signalling telecommunication traffic wavelength division
multiplexing

Non-controlled Indexing

DWDM IEEE Internet Engineering Task Force Optical Interworking Forum all-optical network analytical
approximations call blocking performance client networks dense wavelength division multiplexing efficient transport
services end-to-end control integrated optical network integrated optical network switching architecture interface
methods legacy signaling link utilization network conditions network controller network performance network
signaling nonoptical legacy network traffic optical connection request optical connection signaling optical legacy
network traffic path establishment real-time optical paths resource allocation resource management simulation

results standard organizations transport networks

Author Keywords

Not Available

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June 1999.

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US006643795B1

(12) United States Patent
Nicola et al.
(10) Patent No.: US 6,643,795 B1
(45) Date of Patent: Nov. 4, 2003

(54) CONTROLLER-BASED BI-DIRECTIONAL REMOTE COPY SYSTEM WITH STORAGE SITE FAILOVER CAPABILITY

(75) Inventors: Stephen J. Nicola, Montrose, CO (US); Susan G. Eldington, Colorado Springs, CO (US)

(73) Assignor: Hewlett-Packard Development Company, L.P., Houston, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/538,680
(22) Filed: Mar. 30, 2000

(51) Int. Cl.: G06F 11/00
(52) U.S. Cl.: 714/6; 714/7; 714/11; 714/13

(58) Field of Search: 714/6, 11, 5, 4, 714/7, 13

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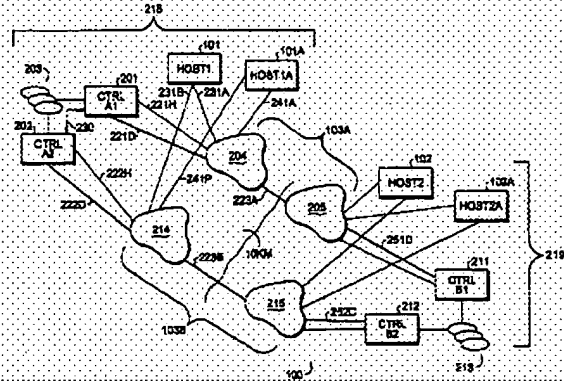
Nicola, Stephen J. et al., U.S. patent application, Dual Redundant Storage Controller Utilizing Tightly Coupled Dual Controller Modules, Ser. No. 08/071,710, Filed Jan. 4, 1993, pp. 1-90.

* cited by examiner
Primary Examiner—Robert Brunelle
Assistant Examiner—Marc Duncan

ABSTRACT

A data replication system having a redundant configuration including dual Fiber Channel fabric links interconnecting each of the components of two data storage sites, wherein each site comprises a host computer and associated data storage array, with redundant array controllers and adapters. The system includes the capability of simultaneous bi-directional remote data replication which permits the system to operate in an "extended cluster" mode, as if each of the remote storage arrays were local relative to the respective remote host. The system further includes the concept of "home" and "alternate" storage nodes, which provides for automatic node failover from a primary to a designated alternate node, without preexisting re-booting of the remote node. Write data transfers are potentially host array-able at both sites upon failure of controllers at one site, the host re-issues the same write on other site.

17 Claims, 18 Drawing Sheets



US-PAT-NO: 6643795

DOCUMENT-IDENTIFIER: US 6643795 B1

TITLE: Controller-based bi-directional remote copy system with storage site failover capability

----- KWIC -----

Brief Summary Text - BSTX (5):

U.S. Pat. No. 5,274,645 (Dec. 28, 1993), to Idleman et al. discloses a dual-active configuration of storage controllers capable of performing failover without the direct involvement of the host. However, the direction taken by Idleman requires a multi-level storage controller implementation. Each controller in the dual-redundant pair includes a two-level hierarchy of controllers. When the first level or host-interface controller of the first controller detects the failure of the second level or device interface controller of the second controller, it re-configures the data path such that the data is directed to the functioning second level controller of the second controller. In conjunction, a switching circuit re-configures the controller-device interconnections, thereby permitting the host to access the storage devices originally connected to the failed second level controller through the operating second level controller of the second controller. Thus, the presence of the first level controllers serves to isolate the host computer from the failover operation, but this isolation is obtained at added controller cost and complexity.

Brief Summary Text - BSTX (10):

U.S. patent application Ser. No. 08/071,710 to Sicola et al., describes a dual-active, redundant storage controller configuration in which each storage controller communicates directly with the host and its own attached devices, the access of which is shared with the other controller. Thus, a failover operation may be executed by one of the storage controller without the assistance of an intermediary controller and without the physical reconfiguration of the data path at the device interface.

Detailed Description Text - DETX (15):

The array controllers 201/202 and 211/212 employed by the present system 100 have two host ports 109 per array controller, for a total of four connections (ports) per pair in the dual redundant configuration of FIG. 3. Each host port 109 preferably has an optical attachment to the switched fabric, for example, a Gigabit Link Module ('GLM') interface at the controller, which connects to a Gigabit Converter ('GBIC') module comprising the switch interface port 107. Switch interconnection ports 306 also preferably comprise GBIC modules. Each pair of array controllers 201/202 and 211/212 (and associated storage array) is also called a storage node (e.g., 301 and 302), and has a unique Fibre Channel Node Identifier. As shown in FIG. 3, array controller pair A1/A2 comprise storage node 301, and array controller pair B1/B2 comprise storage node 302.

US-PAT-NO: 6237028

DOCUMENT-IDENTIFIER: US 6237028 B1

TITLE: Host central processor with associated controller to capture a selected one of a number of memory units via path control commands

----- KWIC -----

Brief Summary Text - BSTX (4):

Workers are also familiar with the practice of associating one or several host central processors (CPUs) with an array of memory units via intermediate controllers (e.g. see U.S. Pat. No. 4,982,324, 4,413,317, 3,889,237, 4,183,084, 3,623,014). And, today, it is not uncommon to operatively associate an array of peripheral storage units with a host computer via an appropriate controller device. FIG. 1 schematically suggests this for a host H and a number of like memory units B, connectible to H via a controller unit C, including suitable interfaces IF, IF' (e.g. see ports 1-4, each connected to a respective, like-numbered drive-port).

Brief Summary Text - BSTX (7):

Now, it may become desirable to mediate the competition between two host-computers to "capture" a selected memory unit (e.g. drive), using certain mediation means. Such a mediation means is the "Shared Memory Interface" (Smi) indicated in FIG. 3, shown in operative relation with eight dual-ported disk drives D0-D7 and a pair of host/controller arrays: host A15 with Controller A and host A17 with Controller B, plus suitable controller inter-faces, IPI-2, IPI-3. Workers should realize that mediation means Smi provides a communication link that allows one controller to request, or transmit, information to, or from, the other controller here via what may be called "direct memory access" (DMA) something that requires special interfaces (e.g. additional special hardware, as "shared memory", SM, and associated interfaces I-A, I-B, (memory typically a dedicated random access memory RAM) and special software). Shared memory, SM, also functions as a common storage unit that can be used to maintain "data path control", i.e. allow/disallow a host to write/read information to/from a selected disk drive.

Brief Summary Text - BSTX (14):

A salient feature of this "Natural Linking" is that it operates "Controller-to-Controller", using only a disk drive as its link, i.e. linking via means which are already part of the system (e.g. here only via a disk drive normally coupled to a M-9730 Controller, plus the "standard" IPI-2 interface normally used by this Controller). That is, here, the inter-controller linkage is "natural", using an already-present disk drive unit via an IPI-2 interface which is normally used for disk control or read/write commands. This way, one controller can now, use its normal (natural) interface to communicate with the other controller, --both controllers being coupled to the two ports of each



United States Patent
 Jackson (10) Patent No.: US 6,237,028 B1
 (45) Date of Patent: *May 22, 2001

(54) **HOST CENTRAL PROCESSOR WITH ASSOCIATED CONTROLLER TO CAPTURE A SELECTED ONE OF A NUMBER OF MEMORY UNITS VIA PATH CONTROL COMMANDS**

(73) **Inventor:** Gary Edward Jackson, Lake Forest, CA (US)

(73) **Assignee:** Unisys Corporation, Blue Bell, PA (US)

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.
 This patent is subject to a terminal disclaimer.

(21) **Appl. No.:** 09/152,692

(22) **Filed:** Sep. 2, 1998

Related U.S. Application Data

(62) Division of application No. 08/650,645, filed on May 2, 1997, now Pat. No. 5,812,782, which is a division of application No. 08/635,052, filed on Mar. 27, 1994, now Pat. No. 5,333,102, which is a division of application No. 07/945,967, filed on Sep. 24, 1992, now Pat. No. 5,201,920.

(51) **Int. Cl.** G06F 12/02; G06F 12/14

(52) **U.S. Cl.** 709/214; 709/210; 710/5; 710/6

(58) **Field of Search** 709/214; 210; 710/5, 36

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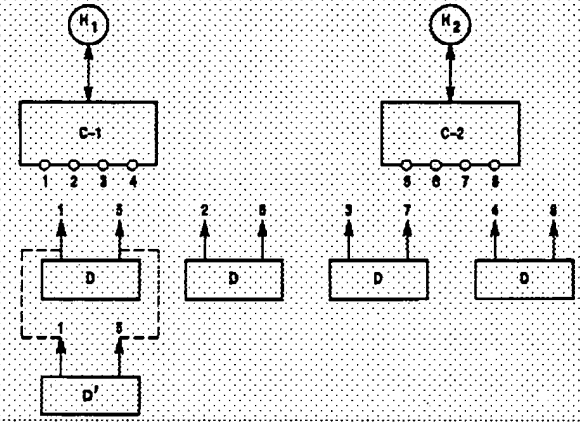
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Primary Examiner—Thomas C. Lee
Assistant Examiner—Rahmat Perveen
(71) Attorney, Agent, or Firm—Mark T. Surr

(57) **ABSTRACT**

A plurality of data processing systems, each of the data processing systems having a host central processor suit to associated controller including memory, both of the data processing systems to be cooperatively associated with a number of disk drive memory units, each of the disk drive memory unit coupled to both said controllers. Either one of the host central processors can appropriate any one of the disk drive memory units as a selected disk drive memory unit by propagating path-control data to the memory in both of the controllers and in the selected disk drive memory unit.

3 Claims, 7 Drawing Sheets



US-PAT-NO: 5630169

DOCUMENT-IDENTIFIER: US 5630169 A

TITLE: Apparatus for a host central processor with associated controller to capture a selected one of a number of memory units via path control commands

----- KWIC -----

Brief Summary Text - BSTX (4):

Workers are also familiar with the practice of associating one or several host central processors (CPUs) with an array of memory units via intermediate controllers (e.g. see U.S. Pat. Nos. 4,962,324, 4,413,317, 3,889,237, 4,183,084, 3,623,014). And, today, it is not uncommon to operatively associate an array of peripheral storage units with a host computer via an appropriate controller device. FIG. 1 schematically suggests this for a host H and a number of like memory units M, connectible to H via a controller unit C, including suitable interfaces IF, IF' (e.g. see ports 1-4, each connected to a respective, like-numbered drive-port).

Brief Summary Text - BSTX (7):

Now, it may become desirable to mediate the competition between two host-computers to "capture" a selected memory unit (e.g. drive), using certain mediation means. Such a mediation means is the "Shared Memory Interface" (SMI) indicated in FIG. 3, shown in operative relation with eight dual-ported disk drives D0-D7 and a pair of host/controller arrays: host A16 with Controller A and host A17 with Controller B, plus suitable controller inter-faces, IPI-2, IPI-3. Workers should realize that mediation means SMI provides a communication link that allows one controller to request, or transmit, information to, or from, the other controller there via what may be called "direct memory access" (DMA) something that requires special interfaces (e.g. additional special hardware, as "shared memory", SM, and associated interfaces I-A, I-B, (memory typically a dedicated random access memory RAM) and special software). Shared memory, SM, also functions as a common storage unit that can be used to maintain "data path control": i.e. allow/disallow a host to write/read information to/from a selected disk drive.

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US 5630169A

United States Patent

Jackson

(11) Patent Number: 5,630,169
(45) Date of Patent: *May 13, 1997

(54) APPARATUS FOR A HOST CENTRAL PROCESSOR WITH ASSOCIATED CONTROLLER TO CAPTURE A SELECTED ONE OF A NUMBER OF MEMORY UNITS VIA PATH CONTROL COMMANDS

(75) Inventor: Gary E. Jackson, Lake Perris, Calif.
(73) Assignee: Celisys Corporation, Blue Bell, Pa.

(*) Notice: The term of this patent shall not extend beyond the expiration date of Pat. No. 5,364,926.

(21) Appl. No.: 628,663
(22) Filed: Mar. 23, 1996

Related U.S. Application Data

(52) Division of Ser. No. 949,597, Sep. 24, 1992, Pat. No. 5,364,926.
(51) Int. Cl.⁶ G06F 13/00; G06F 13/14
(52) U.S. Cl. 395/635; 395/636; 395/475; 395/439; 395/200.01
(58) Field of Search 395/625, 636, 395/475, 200.01, 725, 439

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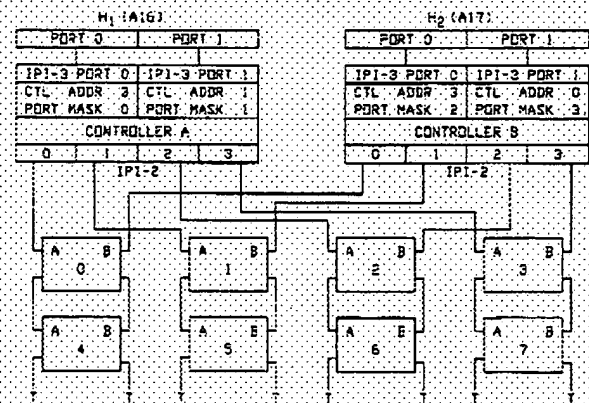
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Primary Examiner—Thomas C. Leo
Assistant Examiner—Rafaela Perveen Krick
Attorney Agent or Firm—John I. McCormack, Mark T. Starr

ABSTRACT

A pair of data processing systems, each of the data processing system having a host central processor and an associated controller including memory, both of the data processing systems to be cooperatively associated with a number of disk drive memory units, each of the disk drive memory unit coupled to both said controllers. Either one of the host central processors can appropriate any one of the disk drive memory units as a selected disk drive memory unit by propagating path-control-data to the memory in both of the controllers and in the selected disk drive memory unit.

3 Claims, 7 Drawing Sheets



US-PAT-NO: 4791629

DOCUMENT-IDENTIFIER: US 4791629 A

TITLE: Communications switching system

----- KWIC -----

Detailed Description Text - DETX (47):

Data values are stored into SE buffer memory which are read by the SEP 64 and stored into frame space. These values include the next intercontroller corresponding address, the link input and output channel pointer, and data values stored in the IBOFIPO. Values in the IBOFIPO can be any values that are in frame space including corresponding addresses, time slot registers, link control and codec enable etc.

Detailed Description Text - DETX (151):

The controller provides a means of controlling communication between the Xbus 23 and the digital stations or analog interfaces to which each controller is coupled. Each controller provides storage for incoming and outgoing data as well as switching services for the individual lines coupled to each controller. The controllers are shown in more detail in FIG. 2. Each controller includes a buffer and latch 41 coupled through line 43 to microprocessor 29. The processor 29 is coupled through an address decoder 69 to buffer 41 and to a memory consisting of dynamic RAM 49, static RAM 38, and EPROM 37. The processor 29 is also coupled through line 46 to a memory page control 39. The processor 29 is coupled through line 44 directly to the dynamic RAM 40, static RAM 38, and eeprom 37. Coupled to the static RAM 38, is a standby power block 30 which provides battery backup during power failure. The clock receiver is coupled to the clock bus 22, switching element 32 and interface element 33. Power is supplied through a DC voltage regulator 34 and a power up/down circuit 31 provided on each controller sequences the activation and deactivation of the microprocessor 29, the SE 32, and the static RAM 38. The switching element 32 is coupled to the interface element 33. The interface element is coupled to the Xbus 23 through a transceiver 36. The interface element 33 is also coupled to digital station interfaces and to analog device interfaces through serial data bus 42, link/codec select line 70, and link control signal line 71.

Detailed Description Text - DETX (176):

The processor buffer consists of a double buffering scheme which is similar to the link/codec buffer and Xbus buffer. The buffer consists of two buffers 54A and 54B with each having an input portion and an output portion. These buffers are memory mapped into the address space of the processor 29 so that the real time code has access to one of the buffers at a particular time while the SEP 64 will process information in the other buffer. The processor 29 access and SEP 64 switch buffers every millisecond (superframe). This means that every 125 microseconds only one byte of link control information and one byte of intercontroller information is swapped. A total of one millisecond is

[11] Patent Number: 4,791,629

[45] Date of Patent: Dec. 13, 1988

Attorney, Agent, or Firm--Blakely, Sokoloff, Taylor & Zafman

[57] ABSTRACT

[57] ABSTRACT

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[57] ABSTRACT

[57] ABSTRACT

[57] ABSTRACT

[57] ABSTRACT

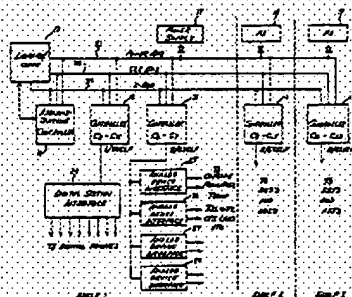
[57] ABSTRACT

[57] ABSTRACT

[57] ABSTRACT

[57] ABSTRACT

16 Claims, 15 Drawing Sheets



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Search Results - Record(s) 1 through 6 of 6 returned.

☐ 1. Document ID: US 6381674 B2

L1: Entry 1 of 6

File: USPT

Apr 30, 2002

US-PAT-NO: 6381674

DOCUMENT-IDENTIFIER: US 6381674 B2

TITLE: Method and apparatus for providing centralized intelligent cache between multiple data controlling elements

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw Desc	Image
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☐ 2. Document ID: US 5790775 A

L1: Entry 2 of 6

File: USPT

Aug 4, 1998

US-PAT-NO: 5790775

DOCUMENT-IDENTIFIER: US 5790775 A

TITLE: Host transparent storage controller failover/failback of SCSI targets and associated units

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw Desc	Image
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☐ 3. Document ID: US 5630169 A

L1: Entry 3 of 6

File: USPT

May 13, 1997

US-PAT-NO: 5630169

DOCUMENT-IDENTIFIER: US 5630169 A

TITLE: Apparatus for a host central processor with associated controller to capture a selected one of a number of memory units via path control commands

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWIC	Draw Desc	Image
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☐ 4. Document ID: US 5530845 A

L1: Entry 4 of 6

File: USPT

Jun 25, 1996

US-PAT-NO: 5530845

DOCUMENT-IDENTIFIER: US 5530845 A

**** See image for Certificate of Correction ****

TITLE: Storage control subsystem implemented with an application program on a computer

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	Image
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☐ 5. Document ID: US 5504926 A

L1: Entry 5 of 6

File: USPT

Apr 2, 1996

US-PAT-NO: 5504926

DOCUMENT-IDENTIFIER: US 5504926 A

TITLE: Method for a host central processor and its associated controller to capture the selected one of a number of memory units via path control commands

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	Image
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☐ 6. Document ID: US 4791629 A

L1: Entry 6 of 6

File: USPT

Dec 13, 1988

US-PAT-NO: 4791629

DOCUMENT-IDENTIFIER: US 4791629 A

TITLE: Communications switching system

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw Desc	Image
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4791629.pn. or 5504926.pn. or 5530845.pn. or 5630169.pn. or 5790775.pn. or 6381674.pn.	6

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